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IN THE UNI[illegible] STATES PATENT AND TRADEMA[illegible] OFFICE

65705 U.S. PTO 07/29/97

[illegible]ent Application of: Leonard Forbes et al.

DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY A[illegible]
METHODS OF FABRICATION AND USE
303.356US1

65705 U.S. PTO 08/902133 07/29/97

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DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY AND METHODS OF FABRICATION AND USE

Cross Reference To Related Applications

This application is related to the following co-pending, commonly assigned U.S. patent applications: "DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR," serial number __________, "DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE," serial number __________, "CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS," serial number __________, "SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS," serial number __________, "TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE," serial number __________, and "TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE," each of which is filed on even date herewith, and each of which disclosure is herein incorporated by reference.

Field of the Invention

The present invention relates generally to integrated circuit technology, including dynamic random access memories (DRAMs) and electrically erasable and programmable read only memories (EEPROMS), and particularly to a floating gate transistor memory that is dynamically electrically alterable and programmable, and methods of fabrication and use.

Background of the Invention

Dynamic random access memories (DRAMs) are data storage devices that store data as charge on a storage capacitor. A DRAM typically includes an array of memory

cells. Each memory cell includes a storage capacitor and an access transistor for transferring charge to and from the storage capacitor. Each memory cell is addressed by a word line and accessed by a bit line. The word line controls the access transistor such that the access transistor controllably couples and decouples the storage capacitor to and from the bit line for writing and reading data to and from the memory cell.

The storage capacitor must have a capacitance that is large enough to retain a charge sufficient to withstand the effects of parasitic capacitances, noise due to circuit operation, and access transistor reverse-bias junction leakage currents between periodic data refreshes. Such effects can result in erroneous data. Obtaining a large capacitance typically requires a storage capacitor having a large area. However, a major goal in DRAM design is to minimize the area of a DRAM memory cell to allow cells to be more densely packed on an integrated circuit die so that more data can be stored on smaller integrated circuits.

In achieving the goal of increasing DRAM array capacity by increasing cell density, the sufficient capacitance levels of the DRAM storage capacitors must be maintained. A "stacked storage cell" design can increase the cell density to some degree. In this technique, two or more capacitor conductive plate layers, such as polycrystalline silicon (polysilicon or poly), are deposited over a memory cell access transistor on a semiconductor wafer. A high dielectric constant material is sandwiched between these capacitor plate layers. Such a capacitor structure is known as a stacked capacitor cell (STC) because the storage capacitor plates are stacked on top of the access transistor. However, formation of stacked capacitors typically requires complicated process steps. Stacked capacitors also typically increase topographical features of the integrated circuit die, making subsequent lithography and processing, such as for interconnection formation, more difficult. Alternatively, storage capacitors can be formed in deep trenches in the semiconductor substrate, but such trench storage capacitors also require additional process complexity. There is a need in the art to further increase memory storage density without adding process complexity or additional topography.

Electrically erasable and programmable read only memories (EEPROMs) provide nonvolatile data storage. EEPROM memory cells typically use field-effect transistors (FETs) having an electrically isolated (floating) gate that affects conduction between source and drain regions of the FET. A gate dielectric is interposed between the floating gate and an underlying channel region between source and drain regions. A control gate is provided adjacent to the floating gate, separated therefrom by an intergate dielectric.

In such memory cells, data is represented by charge stored on the polysilicon floating gates, such as by hot electron injection or Fowler-Nordheim tunneling during a write operation. Fowler-Nordheim tunneling is typically used to remove charge from the polysilicon floating gate during an erase operation. However, the relatively large electron affinity of the polysilicon floating gate presents a relatively large tunneling barrier energy at its interface with the underlying gate dielectric. The large tunneling barrier energy provides longer data retention times than realistically needed. For example, a data charge retention time at 85° C is estimated to be in millions of years for some floating gate memory devices. The large tunneling barrier energy also increases the voltages and time needed to store and remove charge to and from the polysilicon floating gate. "Flash" EEPROMs, which have an architecture that allows the simultaneous erasure of many floating gate transistor memory cells, require even longer erasure times to accomplish this simultaneous erasure. The large erasure voltages needed can result in hole injection into the gate dielectric. This can cause erratic overerasure, damage to the gate dielectric, and introduction of trapping states in the gate dielectric. The high electric fields that result from the large erasure voltages can also result in reliability problems, leading to device failure. There is a need in the art to obtain floating gate transistors that allow the use of lower programming and erasure voltages and shorter programming and erasure times.

Summary of the Invention

The present invention includes a memory cell that allows the use of lower programming and erasure voltages and shorter programming and erasure times by providing a storage electrode for storing charge and providing an adjacent insulator having a barrier energy with the storage electrode of less than approximately 3.3 eV. According to one aspect of the invention, the barrier energy can be established at a predetermined value by selecting various materials for the storage electrode and the insulator, such as to obtain a desired data charge retention time, an erase time, or an erase voltage. In one embodiment, the insulator has a larger electron affinity than silicon dioxide. In another embodiment, the storage electrode has a smaller electron affinity than polycrystalline silicon.

In one embodiment, the memory cell includes a floating gate transistor, having a barrier energy between the floating gate and an insulator of less than approximately 3.3 eV, such as obtained by selecting the materials of the floating gate and the insulator. According to another aspect of the present invention, the transistor is adapted for dynamic refreshing of charge stored on the floating gate. A refresh circuit allows dynamic refreshing of charge stored on the floating gate. The barrier energy can be lowered to a desired value by selecting the appropriate material composition of the floating gate. As a result, lower programming and erasure voltages and shorter programming and erasure times are obtained.

Another aspect of the present invention provides a method of using a floating gate transistor having a barrier energy of less than approximately 3.3 eV at an interface between a floating gate electrode and an adjacent insulator. Data is stored by changing the charge of the floating gate. Data is refreshed based on a data charge retention time established by the barrier energy. Data is read by detecting a conductance between a source and a drain. The large transconductance gain of the memory cell of the present invention provides a more easily detected signal and reduces the required data storage capacitance value and memory cell size when compared to a conventional dynamic random access memory (DRAM) cell.

The present invention also includes a method of forming a floating gate transistor. Source and drain regions are formed. Materials are selected for a floating gate and a gate insulator such that a barrier energy at an interface therebetween is less than approximately 3.3 eV. A gate insulator is formed from the gate insulator material. A floating gate is formed from the gate material, such that the floating gate is isolated from conductors and semiconductors. According to one aspect of the present invention, the floating gate and gate insulator materials are selected based on a desired data charge retention time. If the charge stored on the floating gate is refreshed, the floating gate and gate insulator materials can be selected to obtain a relatively short data charge retention time, thereby obtaining the advantages of shorter write/programming and erase times. The shorter write/programming and erase times make operation of the present memory speed competitive with a DRAM.

The present invention also includes a memory device that is capable of providing short programming and erase times, low programming and erase voltages, and lower electric fields in the memory cell for improved reliability. The memory device includes a plurality of memory cells. Each memory cell includes a transistor. Each transistor includes a source region, a drain region, a channel region between the source and drain regions, and a floating gate that is separated from the channel region by an insulator. An interfacial barrier energy between the floating gate and the insulator is less than approximately 3.3 eV. The transistor also includes a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric. The memory device includes flash electrically erasable and programmable read only memory (EEPROM), dynamic random access memory (DRAM), and dynamically electrically alterable and programmable read only memory (DEAPROM) embodiments.

The memory cell of the present invention, having a barrier energy between the floating electrode and the insulator that is lower than the barrier energy between polysilicon and SiO_2, provides large transconductance gain, an easily detected signal, and reduces the required data storage capacitance value and memory cell size. The lower barrier energy increases tunneling current and also advantageously reduces the

voltage required for writing and erasing the floating gate transistor memory cells. For example, conventional polysilicon floating gate transistors typically require complicated and noisy on-chip charge pump circuits to generate the large erasure voltage, which typically far exceeds other voltages required on the integrated circuit. The present invention allows the use of lower erasure voltages that are more easily provided by simpler on-chip circuits. Reducing the erasure voltage also lowers the electric fields, minimizing reliability problems that can lead to device failure, and better accommodating downward scaling of device dimensions. Alternatively, the thickness of the gate insulator can be increased from the typical thickness of a silicon dioxide gate insulator to improve reliability or simplify processing, since the lower barrier energy allows easier transport of charge across the gate insulator by Fowler-Nordheim tunneling.

According to another aspect of the invention, the shorter retention time of data charges on the floating electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. By decreasing the data charge retention time and periodically refreshing the data, the write and erase operations can be several orders of magnitude faster. In this respect, the memory operates similar to a memory cell in DRAM, but avoids the process complexity, additional space needed, and other limitations of forming stacked or trench DRAM capacitors.

The memory cell of the present invention can be made smaller than a conventional DRAM memory cell. Moreover, because the storage capacitor of the present invention is integrally formed as part of the transistor, rather than requiring complex and costly non-CMOS stacked and trench capacitor process steps, the memory of the present invention should be cheaper to fabricate than DRAM memory cells, and should more easily scale downward as CMOS technology advances.

Brief Description of the Drawings

In the drawings, like numerals describe substantially similar components throughout the several views.

Figure **1** is a simplified schematic/block diagram illustrating generally one embodiment of a memory including reduced barrier energy floating electrode memory cells.

Figure **2** is a cross-sectional view that illustrates generally a floating gate transistor embodiment of a memory cell provided by the present invention.

Figure **3** is an energy band diagram that illustrates generally conduction band energy levels in a floating gate transistor provided by the present invention.

Figure **4** is a graph comparing barrier energy vs. tunneling distance for a conventional floating gate transistor and one embodiment of a the present invention having a lower barrier energy.

Figure **5** is a graph that illustrates generally the relationship between Fowler-Nordheim tunneling current density vs. the barrier energy Φ_{GI} at various parameterized values $E_1 < E_2 < E_3$ of an electric field.

Figure **6** illustrates generally how the barrier energy affects the time needed to perform write and erase operations by Fowler-Nordheim tunneling for a particular voltage.

Figure **7** is a graph that illustrates generally charge density vs. write/erase time for three different embodiments of a floating gate FET.

Figure **8** is a cross-sectional view, similar to Figure **2**, but having a larger area control gate - floating gate capacitor than the floating gate - substrate capacitor.

Figure **9A** is a schematic diagram, labeled prior art, that illustrates generally a conventional DRAM memory cell.

Figure **9B** is a schematic diagram that illustrates generally one embodiment of a floating gate FET memory cell according to the present invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The present invention discloses a dynamic electrically alterable programmable read only memory (DEAPROM) cell. The memory cell has a floating electrode, which is defined as an electrode that is "electrically isolated" from conductors and semiconductors by an insulator such that charge storage upon and removal from the floating electrode depends upon charge conduction through the insulator. In one embodiment, described below, the floating electrode is a floating gate electrode in a floating gate field-effect transistor, such as used in flash electrically erasable and programmable read only memories (EEPROMs). However, a capacitor or any other structure having a floating electrode and adjacent insulator could also be used according to the techniques of the present invention described below. According to one aspect of the present invention, a barrier energy between the floating electrode and the insulator is

lower than the barrier energy between polycrystalline silicon (polysilicon) and silicon dioxide (SiO_2), which is approximately 3.3 eV. According to another aspect of the present invention, the shorter retention time of data charges on the floating electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. In this respect, the memory operates similar to a memory cell in a dynamic random access memory (DRAM). These and other aspects of the present invention are described in more detail below.

Figure **1** is a simplified schematic/block diagram illustrating generally one embodiment of a memory **100** according to one aspect of the present invention, in which reduced barrier energy floating electrode memory cells are incorporated. Memory **100** is referred to as a dynamic electrically alterable programmable read only memory (DEAPROM) in this application, but it is understood that memory **100** possesses certain characteristics that are similar to DRAMs and flash EEPROMs, as explained below. For a general description of how a flash EEPROM operates, see B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993), which is incorporated herein by reference. Memory **100** includes a memory array **105** of multiple memory cells **110**. Row decoder **115** and column decoder **120** decode addresses provided on address lines **125** to access the addressed memory cells in memory array **105**. Command and control circuitry **130** controls the operation of memory **100** in response to control signals received on control lines **135** from a processor **140** or other memory controller during read, write, refresh, and erase operations. Command and control circuitry **130** includes a refresh circuit for periodically refreshing the data stored on floating gate transistor or other floating electrode memory cells **110**. Voltage control **150** provides appropriate voltages to the memory cells during read, write, refresh, and erase operations. Memory **100**, as illustrated in Figure **1**, has been simplified for the purpose of illustrating the present invention and is not intended to be a complete description. Only the substantial differences between DEAPROM memory **100** and conventional DRAM and flash EEPROM memories are discussed below.

Figure **2** is a cross-sectional view that illustrates generally, by way of example, but not by way of limitation, one floating gate transistor embodiment of a memory cell **110**. Other structural arrangements of floating gate transistors are included within the present invention. Also included are any memory cells that incorporate a floating electrode (such as a floating electrode capacitor) having, at an interface between the floating electrode an adjacent insulator, a barrier energy that is less than the barrier energy at a polysilicon-SiO_2 interface. In the embodiment of Figure **2**, memory cell **110** includes a floating gate FET **200**, which is illustrated as an n-channel FET, but understood to include a p-channel FET embodiment as well.

FET **200** includes a source **205**, a drain **210**, a floating gate **215** electrode, and a control gate **220** electrode. A gate insulator **225** is interposed between floating gate **215** and substrate **230**. An intergate insulator **235** is interposed between floating gate **215** and control gate **220**. In one embodiment, substrate **230** is a bulk semiconductor, such as silicon. In another embodiment, substrate **230** includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a semiconductor-on-insulator (SOI) or other thin film transistor technology. Source **205** and drain **210** are formed by conventional complementary metal-oxide-semiconductor (CMOS) processing techniques. Source **205** and drain **210** are separated by a predetermined length for forming an inversion channel **240** therebetween.

Figure **3** is an energy band diagram that illustrates generally the conduction band energy levels in floating gate **215**, gate insulator **225**, and substrate **230**. Electron affinities χ_{215}, χ_{225}, and χ_{230} describe floating gate **215**, gate insulator **225**, and substrate **230**, respectively, when measured with respect to a vacuum level **300**. A barrier energy Φ_{GI}, which describes the barrier energy at the interface between floating gate **215** and gate insulator **225**, is given by a difference in electron affinities, as illustrated in Equation **1**.

$$\Phi_{GI}=\chi_{215}-\chi_{225} \qquad \textbf{(1)}$$

A barrier energy Φ_{SG}, which describes the barrier energy at the interface between substrate **230** and gate insulator **225**, is given by a difference in electron affinities, as illustrated in Equation **2**.

$$\Phi_{SG}=\chi_{230}-\chi_{225} \tag{2}$$

Silicon (monocrystalline or polycrystalline Si) has an electron affinity $\chi_{215} \approx 4.2$ eV. Silicon dioxide (SiO_2) has an electron affinity, χ_{225}, of about 0.9 eV. The resulting barrier energy at a conventional Si-SiO_2 interface between a floating gate and a gate insulator is approximately equal to 3.3 eV. One aspect of the present invention provides a barrier energy Φ_{GI} that is less than the 3.3 eV barrier energy of a conventional Si-SiO_2 interface.

According to one aspect of the invention, the interface between floating gate **215** and gate insulator **225** provides a smaller barrier energy Φ_{GI} than the 3.3 eV barrier energy at an interface between polysilicon and silicon dioxide, such as by an appropriate selection of the material composition of one or both of floating gate **215** and gate insulator **225**. In one embodiment, the smaller barrier energy Φ_{GI} is obtained by forming floating gate **215** from a material having a smaller electron affinity χ_{215} than polysilicon. In one embodiment, for example, polycrystalline or microcrystalline silicon carbide (SiC) is used as the material for forming floating gate **215**. In another embodiment, the smaller barrier energy Φ_{GI} is obtained by forming gate insulator **225** from a material having a higher electron affinity χ_{225} than SiO_2. In one embodiment, for example, amorphous SiC is used as the material for forming gate insulator **225**. In yet another embodiment, the smaller barrier energy Φ_{GI} is obtained by a combination of forming floating gate **215** from a material having a smaller electron affinity χ_{215} than polysilicon and also forming gate insulator **225** from a material having a higher electron affinity χ_{225} than SiO_2.

The smaller barrier energy Φ_{GI} provides current conduction across gate insulator **225** that is easier than for a polysilicon-SiO_2 interface. The present invention includes

any mechanism of providing such easier current conduction across gate insulator **225**, including, but not limited to "hot" electron injection, thermionic emission, Schottky emission, Frenkel-Poole emission, and Fowler-Nordheim tunneling. Such techniques for transporting charge carriers across an insulator, such as gate insulator **225**, are all enhanced by providing a smaller barrier energy Φ_{GI} according to the techniques of the present invention. These techniques allow increased current conduction, current conduction at lower voltages across gate insulator **225** and lower electric fields in gate insulator **225**, shorter data write and erase times, use of a thicker and more reliable gate insulator **225**, and other advantages explained below.

Figure **4** is a graph illustrating generally barrier energy versus tunneling distance for a conventional polysilicon-SiO_2 interface having a 3.3 eV barrier energy. Figure **4** also illustrates barrier energy versus tunneling distance for an interface according to the present invention that has a barrier energy of $\Phi_{GI} \approx 1.08$ eV, which is selected as an illustrative example, and not by way of limitation. The smaller barrier energy Φ_{GI} reduces the energy to which the electrons must be excited to be stored on or removed from the floating gate **215**, such as by thermal emission over the barrier. The smaller barrier energy Φ_{GI} also reduces the distance that electrons have to traverse, such as by Fowler-Nordheim tunneling, to be stored upon or removed from floating gate **215**. In Figure **4**, "do" represents the tunneling distance of a conventional floating gate transistor due to the 3.3 eV barrier energy represented by the dashed line "OLD". The tunneling distance "dn" corresponds to a floating gate transistor according to the present invention and its smaller barrier energy, such as $\Phi_{GI} \approx 1.08$ eV, for example, represented by the dashed line "NEW". Even a small reduction in the tunneling distance results in a large increase in the tunneling probability, as described below, because the tunneling probability is an exponential function of the reciprocal of the tunneling distance.

The Fowler-Nordheim tunneling current density in gate insulator **225**, which is illustrated approximately by Equation **3** below, is described in a textbook by S.M. Sze, "Physics of Semiconductor Devices," John Wiley & Sons, New York (1969), p. 496.

$$J = AE^2 e^{(-\frac{B}{E})} \quad \textbf{(3)}$$

In Equation **3**, J is the current density in units of amperes/cm^2, E is the electric field in gate insulator **225** in units of volts/cm and A and B are constants, which are particular to the material of gate insulator **225**, that depend on the effective electron mass in the gate insulator **225** material and on the barrier energy Φ_{GI}. The constants A and B scale with the barrier energy Φ_{GI}, as illustrated approximately by Equations **4** and **5**, which are disclosed in S.R. Pollack et al., "Electron Transport Through Insulating Thin Films," Applied Solid State Science, Vol. 1, Academic Press, New York, (1969), p. 354.

$$A \alpha (\frac{1}{\Phi_{GI}}) \quad \textbf{(4)}$$

$$B \alpha (\Phi_{GI})^{\frac{3}{2}} \quad \textbf{(5)}$$

For a conventional floating gate FET having a 3.3 eV barrier energy at the interface between the polysilicon floating gate and the SiO_2 gate insulator, A = 5.5 x 10^{-16} amperes/Volt^2 and B = 7.07 x 10^7 Volts/cm, as disclosed in D.A. Baglee, "Characteristics and Reliability of 100 Å Oxides," Proc. 22nd Reliability Symposium, (1984), p. 152. One aspect of the present invention includes selecting a smaller barrier energy Φ_{GI} such as, by way of example, but not by way of limitation, $\Phi_{GI} \approx 1.08$ eV. The constants A and B for $\Phi_{GI} \approx 1.08$ eV can be extrapolated from the constants A and B for the 3.3 eV polysilicon-SiO_2 barrier energy using Equations **4** and **5**. The barrier energy $\Phi_{GI} \approx 1.08$ eV yields the resulting constants A = 1.76 x 10^{-15} amperes/Volt^2 and B = 1.24 x 10^7 Volts/cm.

Figure **5** is a graph that illustrates generally the relationship between Fowler-Nordheim tunneling current density vs. the barrier energy Φ_{GI}, such as at various parameterized values $E_1 < E_2 < E_3$ of an electric field in gate insulator **225**. The tunneling current density increases as electric field is increased. The tunneling current also increases by orders of magnitude as the barrier energy Φ_{GI} is decreased, such as by selecting the materials for floating gate **215** and gate insulator **225** or otherwise reducing the barrier energy Φ_{GI} according to the techniques of the present invention. In particular, Figure **5** illustrates a comparison between tunneling current densities at the 3.3 eV barrier energy of a conventional polysilicon-SiO_2 interface and at the illustrative example barrier energy $\Phi_{GI} \approx 1.08$ eV for which constants A and B were extrapolated above. Reducing the 3.3 eV barrier energy to $\Phi_{GI} \approx 1.08$ eV increases the tunneling current density by several orders of magnitude.

Figure **6** is a conceptual diagram, using rough order of magnitude estimates, that illustrates generally how the barrier energy affects the time needed to perform write and erase operations by Fowler-Nordheim tunneling for a particular voltage, such as across gate insulator **225**. Figure **6** also illustrates how the barrier energy affects data charge retention time, such as on floating gate **215** at a temperature of 250 degrees Celsius. Both write and erase time **600** and data charge retention time **605** are decreased by orders of magnitude as the barrier energy is decreased, according to the present invention, from the conventional polysilicon-SiO_2 interface barrier energy of 3.3 eV to the illustrative example lower barrier energy $\Phi_{GI} \approx 1.08$ eV for which constants A and B were extrapolated above.

The lower barrier energy Φ_{GI} and increased tunneling current advantageously provides faster write and erase times. This is particularly advantageous for "flash" EEPROMs or DEAPROMs in which many floating gate transistor memory cells must be erased simultaneously, requiring a longer time to transport the larger quantity of charge. For a flash EEPROM using a polysilicon floating gate transistor having an underlying SiO_2 gate insulator 225, the simultaneous erasure of a block of memory cells

requires a time that is on the order of milliseconds. The write and erase time of the floating gate FET **200** is illustrated approximately by Equation **6**.

$$t=\int_0^t dt=\int_0^Q \left(\frac{1}{J_{225}-J_{235}}\right)dQ \tag{6}$$

In Equation **6**, t is the write/erase time, J_{225} and J_{235} are the respective tunneling current densities in gate dielectric **225** and intergate dielectric **235**, Q is the charge density in Coulombs/cm^2 on floating gate **215**. Equation **6** is evaluated for a specific voltage on control gate **220** using Equations **7** and **8**.

$$E_{225}=\frac{V_{220}}{\left[d_{225}+d_{235}\left(\frac{\epsilon_{225}}{\epsilon_{235}}\right)\right]-\frac{Q}{\left[\epsilon_{225}+\epsilon_{235}\left(\frac{d_{225}}{d_{235}}\right)\right]}} \tag{7}$$

$$E_{235}=\frac{V_{220}}{\left[d_{235}+d_{225}\left(\frac{\epsilon_{235}}{\epsilon_{225}}\right)\right]+\frac{Q}{\left[\epsilon_{235}+\epsilon_{225}\left(\frac{d_{235}}{d_{225}}\right)\right]}} \tag{8}$$

In Equations **7** and **8**, V_{220} is the voltage on control gate **220**, E_{225} and E_{235} are the respective electric fields in gate insulator **225** and intergate insulator **235**, d_{225} and d_{235} are the respective thicknesses of gate insulator **225** and intergate insulator **235**, and ϵ_{225} and ϵ_{235} are the respective permittivities of gate insulator **225** and intergate insulator **235**.

Figure **7** is a graph that illustrates generally charge density vs. write/erase time for three different embodiments of the floating gate FET **200**, each of which have a polysilicon floating gate **215**, by way of illustrative example. Line **700** illustrates generally, by way of example, but not by way of limitation, the charge density vs. write/erase time obtained for a floating gate FET **200** having a 100 Å SiO_2 gate insulator **225** and a 150 Å SiO_2 (or thinner oxynitride equivalent capacitance) intergate insulator **235**.

Line **705** is similar to line **700** in all respects except that line **705** illustrates a floating gate FET **200** in which gate insulator **225** comprises a material having a higher electron affinity χ_{225} than SiO_2, thereby providing a lower barrier energy Φ_{GI} at the interface between polysilicon floating gate **215** and gate insulator **225**. The increased tunneling current results in shorter write/erase times than those illustrated by line **700**.

Line **710** is similar to line **705** in all respects except that line **710** illustrates a floating gate FET **200** in which gate insulator **225** has a lower barrier energy Φ_{GI} than for line **705**, or intergate insulator **235** has a higher permittivity ϵ_{235} than for line **705**, or control gate **220** has a larger area than floating gate **215**, such as illustrated by way of example by the floating gate FET **800** in the cross-sectional view of Figure **8**. As seen in Figure **8**, the area of a capacitor formed by the control gate **220**, the floating gate **215**, and the intergate insulator **235** is larger than the area of a capacitor formed by the floating gate **215**, the gate insulator **225**, and the inversion channel **240** underlying gate insulator **225**. Alternatively, or in combination with the techniques illustrated in Figure **8**, the intergate insulator **235** can have a higher permittivity than the permittivity of silicon dioxide.

As illustrated in Figure 7, the barrier energy Φ_{GI} can be selected to reduce the write/erase time. In one embodiment, by way of example, but not by way of limitation, the barrier energy Φ_{GI} is selected to obtain a write/erase time of less than or equal to 1 second, as illustrated in Figure 7. In another embodiment, by way of example, but not by way of limitation, the barrier energy Φ_{GI} is selected to obtain a write/erase time of

less than or equal to 1 millisecond, as illustrated in Figure **7**. Other values of write/erase time can also be obtained by selecting the appropriate value of the barrier energy Φ_{GI}.

The lower barrier energy Φ_{GI} and increased tunneling current also advantageously reduces the voltage required for writing and erasing the floating gate transistor memory cells **110**. For example, conventional polysilicon floating gate transistors typically require complicated and noisy on-chip charge pump circuits to generate the large erasure voltage, which typically far exceeds other voltages required on the integrated circuit. The present invention allows the use of lower erasure voltages that are more easily provided by simpler on-chip circuits. Reducing the erasure voltage also lowers the electric fields, minimizing reliability problems that can lead to device failure, and better accommodating downward scaling of device dimensions. In one embodiment, the barrier energy Φ_{GI} is selected, as described above, to obtain an erase voltage of less than the 12 Volts required by typical EEPROM memory cells.

Alternatively, the thickness of the gate insulator **225** can be increased from the typical thickness of a silicon dioxide gate insulator to improve reliability or simplify processing, since the lower barrier energy Φ_{GI} allows easier transport of charge across the gate insulator **225** by Fowler-Nordheim tunneling.

The lower barrier energy Φ_{GI} also decreases the data charge retention time of the charge stored on the floating gate **215**, such as from increased thermal excitation of stored charge over the lower barrier Φ_{GI}. However, conventional polysilicon floating gates and adjacent SiO_2 insulators (e.g., 90 Å thick) have a data charge retention time estimated in the millions of years at a temperature of 85 degrees C, and estimated in the 1000 hour range even at extremely high temperatures such as 250 degrees C. Since such long data charge retention times are longer than what is realistically needed, a shorter data charge retention time can be accommodated in order to obtain the benefits of the smaller barrier energy Φ_{GI}. In one embodiment of the present invention, by way of example, but not by way of limitation, the barrier energy Φ_{GI} is lowered to $\Phi_{GI} \approx 1.08$ eV by appropriately selecting the composition of the materials of floating gate **215** and gate insulator **225**, as described below. As a result, an estimated data charge retention

time of approximately 40 seconds at a high temperature, such as 250 degrees C, is obtained.

According to one aspect of the present invention, the data stored on the DEAPROM floating gate memory cell **110** is periodically refreshed at an interval that is shorter than the data charge retention time. In one embodiment, for example, the data is refreshed every few seconds, such as for an embodiment having a high temperature retention time of approximately 40 seconds for $\Phi_{GI} \approx 1.08$ eV. The exact refresh rate can be experimentally determined and tailored to a particular process of fabricating the DEAPROM. By decreasing the data charge retention time and periodically refreshing the data, the write and erase operations can be several orders of magnitude faster, as described above with respect to Figure **7**.

Figures **9A** and **9B** are schematic diagrams that respectively illustrate generally a conventional DRAM memory cell and the present invention's floating gate FET **200** embodiment of memory cell **110**. In Figure **9A**, the DRAM memory cell includes an access FET **900** and stacked or trench storage capacitor **905**. Data is stored as charge on storage capacitor **905** by providing a control voltage on control line **910** to activate FET **900** for conducting charge. Data line **915** provides a write voltage to conduct charge across FET **900** for storage on storage capacitor **905**. Data is read by providing a control voltage on control line **910** to activate FET **900** for conducting charge from storage capacitor **905**, thereby incrementally changing a preinitialized voltage on data line **915**. The resulting small change in voltage on data line **915** must be amplified by a sense amplifier for detection. Thus, the DRAM memory cell of Figure **9A** inherently provides only a small data signal. The small data signal is difficult to detect.

In Figure **9B**, the DEAPROM memory cell **110** according to the present invention includes floating gate FET **200**, having source **205** coupled to a ground voltage or other reference potential. Data is stored as charge on floating gate **215** by providing a control voltage on control line **920** and a write voltage on data line **925** for hot electron injection or Fowler-Nordheim tunneling. This is similar to conventional

EEPROM techniques, but advantageously uses the reduced voltages and/or a shorter write time of the present invention.

The DEAPROM memory cell **110** can be smaller than the DRAM memory cell of Figure **9A**, allowing higher density data storage. The leakage of charge from floating gate **215** can be made less than the reverse-bias junction leakage from storage capacitor **905** of the DRAM memory cell by tailoring the barrier energy Φ_{GI} according to the techniques of the present invention. Also, the DEAPROM memory cell advantageously uses the large transconductance gain of the floating gate FET **200**. The conventional DRAM memory cell of Figure **9A** provides no such gain; it is read by directly transferring the data charge from storage capacitor **905**. By contrast, the DEAPROM memory cell **110** is read by placing a read voltage on control line **920**, and detecting the current conducted through FET **200**, such as at data line **925**. The current conducted through FET **200** changes significantly in the presence or absence of charge stored on floating gate **215**. Thus, the present invention advantageously provides an large data signal that is easy to detect, unlike the small data signal provided by the conventional DRAM memory cell of Figure **9A**.

For example, the current for floating gate FET **200** operating in the saturation region can be approximated by Equation **9**.

$$I_{DS}=\frac{1}{2}\mu C_o(\frac{W}{L})(V_G-V_T)^2 \qquad \textbf{(9)}$$

In Equation **9**, I_{DS} is the current between drain **210** and source **205**, C_o is the capacitance per unit area of the gate insulator **225**, W/L is the width/length aspect ratio of FET **200**, V_G is the gate voltage applied to control gate **220**, and V_T is the turn-on threshold voltage of FET **200**.

For an illustrative example, but not by way of limitation, a minimum-sized FET having W/L=1, can yield a transconductance gain of approximately 71 μA/Volt for a typical process. In this illustrative example, sufficient charge is stored on floating gate

215 to change the effective threshold voltage V_T by approximately 1.4 Volts, thereby changing the current I_{DS} by approximately 100 microamperes. This significant change in current can easily be detected, such as by sampling or integrating over a time period of approximately 10 nanoseconds, for example, to obtain a detected data charge signal of 1000 fC. Thus, the DEAPROM memory cell **110** is capable of yielding a detected data charge signal that is approximately an order of magnitude larger than the typical 30 fC to 100 fC data charges typically stored on DRAM stacked or trench capacitors. Since DEAPROM memory cell **110** requires a smaller capacitance value than a conventional DRAM memory cell, DEAPROM memory cell **110** can be made smaller than a conventional DRAM memory cell. Moreover, because the CMOS-compatible DEAPROM storage capacitor is integrally formed as part of the transistor, rather than requiring complex and costly non-CMOS stacked and trench capacitor process steps, the DEAPROM memory of the present invention should be cheaper to fabricate than DRAM memory cells, and should more easily scale downward as CMOS technology advances.

Amorphous SiC Gate Insulator Embodiment

In one embodiment, the present invention provides a DEAPROM having a storage element including a gate insulator **225** that includes an amorphous silicon carbide (a-SiC). For example, one embodiment of a memory storage element having an a-SiC gate insulator **225** is described in Forbes et al. U.S. Patent application serial number ______________ entitled CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference. The a-SiC inclusive gate insulator **225** provides a higher electron affinity χ_{225} than the approximately 0.9 eV electron affinity of SiO_2. For example, but not by way of limitation, the a-SiC inclusive gate insulator **225** can provide an electron affinity $\chi_{225} \approx$ 3.24 eV.

An a-SiC inclusive gate insulator **225** can also be formed using other techniques. For example, in one embodiment gate insulator **225** includes a hydrogenated a-SiC material synthesized by ion-implantation of C_2H_2 into a silicon substrate **230**. For example, see G. Comapagnini et al. "Spectroscopic Characterization of Annealed $Si_{1-x}C_x$ Films Synthesized by Ion Implantation," J. of Materials Research, Vol. 11, No. 9, pp. 2269-73, (1996). In another embodiment, gate insulator **225** includes an a-SiC film that is deposited by laser ablation at room temperature using a pulsed laser in an ultrahigh vacuum or nitrogen environment. For example, see A. L. Yee et al. "The Effect of Nitrogen on Pulsed Laser Deposition of Amorphous Silicon Carbide Films: Properties and Structure," J. Of Materials Research, Vol. 11, No. 8, pp. 1979-86 (1996). In another embodiment, gate insulator **225** includes an a-SiC film that is formed by low-energy ion-beam assisted deposition to minimize structural defects and provide better electrical characteristics in the semiconductor substrate **230**. For example, see C. D. Tucker et al. "Ion-beam Assisted Deposition of Nonhydrogenated a-Si:C films," Canadian J. Of Physics, Vol. 74, No. 3-4, pp. 97-101 (1996). The ion beam can be generated by electron cyclotron resonance from an ultra high purity argon (Ar) plasma.

In another embodiment, gate insulator **225** includes an a-SiC film that is synthesized at low temperature by ion beam sputtering in a reactive gas environment with concurrent ion irradiation. For example, see H. Zhang et al., "Ion-beam Assisted Deposition of Si-Carbide Films," Thin Solid Films, Vol. 260, No. 1, pp. 32 -37 (1995). According to one technique, more than one ion beam, such as an Ar ion beam, are used. A first Ar ion beam is directed at a Si target material to provide a Si flux for forming SiC gate insulator **225**. A second Ar ion beam is directed at a graphite target to provide a C flux for forming SiC gate insulator **225**. The resulting a-SiC gate insulator **225** is formed by sputtering on substrate **230**. In another embodiment, gate insulator **225** includes an SiC film that is deposited on substrate **230** by DC magnetron sputtering at room temperature using a conductive, dense ceramic target. For example, see S. P. Baker et al. "D-C Magnetron Sputtered Silicon Carbide," Thin Films, Stresses and Mechanical Properties V. Symposium, pp. Xix+901, 227-32 (1995). In another

embodiment, gate insulator **225** includes a thin a-$Si_{1-x}C_x$:H film that is formed by HF plasma ion sputtering of a fused SiC target in an Ar-H atmosphere. For example, see N. N. Svirkova et al. "Deposition Conditions and Density-of-States Spectrum of a-$Si_{1-x}C_x$:H Films Obtained by Sputtering," Semiconductors, Vol. 28, No. 12, pp. 1164-9 (1994). In another embodiment, radio frequency (RF) sputtering is used to produce a-SiC films. For example, see Y. Suzaki et al. "Quantum Size Effects of a-Si(:H)/a-SiC(:H) Multilayer Films Prepared by RF Sputtering," J. Of Japan Soc. Of Precision Engineering, Vol. 60, No. 3, pp. 110-18 (1996). Bandgaps of a-Si, a-SiC, a-Si:H, and a-SiC:H have been found to be 1.22 eV, 1.52 eV, 1.87 eV, and 2.2 eV respectively.

In another embodiment, gate insulator **225** is formed by chemical vapor deposition (CVD) and includes an a-SiC material. According to one technique, gate insulator **225** includes a-$Si_{1-x}C_x$:H deposited by plasma enhanced chemical vapor deposition (PECVD). For example, see I. Pereyra et al. "Wide Gap a-$Si_{1-x}C_x$:H Thin Films Obtained Under Starving Plasma Deposition Conditions," J. Of Non-crystalline Solids, Vol. 201, No. 1-2, pp. 110-118 (1995). According to another technique, mixed gases of silane and methane can be used to form a-$Si_{1-x}C_x$:H gate insulator **225**. For example, the source gas can include silane in methane with additional dilution in hydrogen. In another embodiment, gate insulator **225** includes a clean a-$Si_{1-x}C_x$ material formed by hot-filament assisted CVD. For example, see A. S. Kumbhar et al. "Growth of Clean Amorphous Silicon Carbon Alloy Films By Hot-Filament Assisted Chemical Vapor Deposition Technique," Appl. Phys. Letters, Vol. 66, No. 14, pp. 1741-3 (1995). In another embodiment, gate insulator **225** includes a-SiC formed on a crystalline Si substrate **230** by inductively coupled plasma CVD, such as at 450 degrees Celsius, which can yield a-SiC rather than epitaxially grown polycrystalline or microcrystalline SiC. The resulting a-SiC inclusive gate insulator **225** can provide an electron affinity $\chi_{225} \approx 3.24$ eV, which is significantly larger than the 0.9 eV electron affinity obtainable from a conventional SiO_2 gate insulator. For example, see J. H. Thomas et al. "Plasma Etching and Surface Analysis of a-SiC:H Films Deposited by Low Temperature Plasma

Enhanced Vapor Deposition," Gas-phase and Surface Chemistry in Electronic Materials Processing Symposium, Materials Research Soc., pp. Xv+556, 445-50 (1994).

Gate insulator **225** can be etched by RF plasma etching using CF_4O_2 in SF_6O_2. Self-aligned source **205** and drain **210** can then be formed using conventional techniques for forming a FET **200** having a floating (electrically isolated) gate **215**, or in an alternate embodiment, an electrically interconnected (driven) gate.

SiC Gate Material Embodiment

In one embodiment, the present invention provides a DEAPROM having a memory cell **110** that includes a FET **200** having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, nanocrystalline, or combination thereof) SiC floating gate **215**. For example, one embodiment of a memory cell **110** that includes a memory storage element having a polycrystalline or microcrystalline SiC floating gate **215** is described in Forbes et al. U.S. Patent application serial number _______________ entitled SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference. The SiC floating gate **215** provides a lower electron affinity $\chi_{215} \approx 3.7$ to 3.8 eV and smaller resulting barrier energy Φ_{GI} than a polysilicon gate material having an electron affinity $\chi_{215} \approx 4.2$ eV. For example, using a SiO_2 gate insulator **225**, a barrier energy $\Phi_{GI} \approx 2.6$ to 2.7 eV is obtained using an SiC floating gate **215**, as compared to a barrier energy $\Phi_{GI} \approx 3.3$ eV for a conventional polysilicon floating gate material at an interface with an SiO_2 gate insulator **225**.

According to one aspect of the invention, floating gate **215** is formed from a silicon carbide compound $Si_{1-x}C_x$, in which the material composition x is varied. One embodiment of a memory storage element having a variable SiC composition floating gate **215** is described in Forbes et al. U.S. Patent application serial number _____________ entitled TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE, filed on the same day as the

present patent application, and which disclosure is herein incorporated by reference. For example, but not by way of limitation, an SiC composition of about $0.75 < x < 1.0$ yields an electron affinity of approximately between $1.7 \text{ eV} < \chi_{215} < -0.4 \text{ eV}$. For an SiO_2 gate insulator **225**, a barrier $0.8 \text{ eV} < \Phi_{GI} < -1.3 \text{ eV}$ is obtained. In one such embodiment, floating gate FET **200** provides a data charge retention time on the order of seconds.

In one embodiment, floating gate **215** is formed by CVD of polycrystalline or microcrystalline SiC, which can be either *in situ* conductively doped during deposition, or conductively doped during a subsequent ion-implantation step. According to one aspect of the invention, for example, floating gate **215** is formed of an SiC film that is deposited using low-pressure chemical vapor deposition (LPCVD). The LPCVD process uses either a hot-wall reactor or a cold-wall reactor with a reactive gas, such as a mixture of $Si(CH_3)_4$ and Ar. Examples of such processes are disclosed in an article by Y. Yamaguchi et al., entitled "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", in the <u>8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers</u>, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995, and in an article by M. Andrieux, et al., entitled "Interface and Adhesion of PECVD SiC Based Films on Metals", in supplement <u>Le Vide Science, Technique et Applications.</u> (France), No. 279, pages 212-214, 1996. In other embodiments, floating gate **215** is formed of an SiC film that is deposited using other techniques such as, for example, enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal chemical vapor deposition (LP-RTCVD), or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy (MBE). Other examples of forming SiC film floating gate **215** include reactive magnetron sputtering, DC plasma discharge, ion-beam assisted deposition, ion-beam synthesis of amorphous SiC films, laser crystallization of amorphous SiC, laser reactive ablation deposition, and epitaxial growth by vacuum anneal. The conductivity of the SiC film of floating gate **215** can be changed by ion

implantation during subsequent process steps, such as during the self-aligned formation of source/drain regions for the n-channel and p-channel FETs.

In one embodiment, patterning and etching the SiC film, together with the underlying gate insulator **225**, forms the resulting individual SiC floating gates **215**. The SiC film is patterned using standard techniques and is etched using plasma etching, reactive ion etching (RIE) or a combination of these or other suitable methods. For example, the SiC film can be etched by RIE in a distributed cyclotron resonance reactor using a SF_6 /O_2 gas mixture using SiO_2 as a mask with a selectivity of 6.5. Such process is known in the art and is disclosed, for example, in an article by F. Lanois, entitled "Angle Etch Control for Silicon Power Devices", which appeared in Applied Physics Letters, Vol 69, No. 2, pages 236-238, July 1996. Alternatively, the SiC film can be etched by RIE using the mixture SF_6 and O_2 and F_2/Ar/O_2. An example of such a process is disclosed in an article by N. J. Dartnell, et al., entitled "Reactive Ion Etching of Silicon Carbide" in Vacuum, Vol. 46, No. 4, pages 349-355, 1955. The etch rate of the SiC film can be significantly increased by using magnetron enhanced RIE. Self-aligned source **205** and drain **210** regions can then be formed using conventional techniques for forming a FET **200** having a floating (electrically isolated) gate **215**, or in an alternate embodiment, an electrically interconnected (driven) gate.

SiOC Gate Material Embodiment

In one embodiment, the present invention provides a DEAPROM having a memory cell 110 that includes a FET **200** having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, or nanocrystalline) silicon oxycarbide (SiOC) floating gate **215**. For example, one embodiment of a memory cell **110** that includes a storage element having a polycrystalline or microcrystalline SiOC floating gate **215** is described in Forbes et al. U.S. Patent application serial number ______________ entitled TRANSISTOR WITH SILICON OXYCARBIDE GATE AND METHODS OF FABRICATION AND USE, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference.

In one embodiment, a material composition w of the $SiO_{(2-2w)}C_w$ floating gate **215** is selected such that floating gate **215** provides a lower electron affinity approximately between $0.9\ eV < \chi_{215} < 3.7\ eV$ and smaller resulting barrier energy Φ_{GI} than a polysilicon gate material having an electron affinity $\chi_{215} \approx 4.2\ eV$. For example, using a SiO_2 gate insulator **225**, a barrier energy approximately between $0\ eV < \Phi_{GI} < 2.8\ eV$ is obtained for an SiOC floating gate **215** as the SiOC composition w varies between $w \approx 1$ (i.e., approximately SiC) and $w \approx 0$ (i.e., approximately SiO_2). By contrast, a conventional polysilicon floating gate material provides a barrier energy $\Phi_{GI} \approx 3.3\ eV$ at an interface with an SiO_2 gate insulator **225**.

In one embodiment floating gate **215** is formed of a monocrystalline, polycrystalline, microcrystalline, or nanocrystalline, SiOC thin film that is CVD deposited, such as by a Two Consecutive Decomposition and Deposition Chamber (TCDDC) system. One such example of depositing microcrystalline SiOC, in the unrelated technological field of solar cell applications, is disclosed in an article by R. Martins et al., entitled "Transport Properties of Doped Silicon Oxycarbide Microcrystalline Films Produced By Spatial Separation Techniques," <u>Solar Energy Materials and Solar Cells</u>, Vol. 41-42, pp. 493-517, June 1996. <u>See</u> <u>also</u> an article by R. Martins et al., entitled "Wide band-gap microcrystalline silicon thin films," <u>Diffusion and Defect Data Part B (Solid State Phenomena)</u>, Vol. 44-46, Pt. 2, pp. 299-346, 1995.

In other embodiments, the SiOC film is deposited using other techniques such as, for example, low pressure chemical vapor deposition (LPCVD). or enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal chemical vapor deposition (LP-RTCVD). The conductivity of the SiOC film floating gate **215** can be changed by ion implantation during subsequent process steps, such as during the self-aligned formation of source/drain regions for the n-channel and p-channel FETs. The SiOC film can be patterned and etched, together with the underlying gate insulator **225**, such as by using plasma etching, reactive ion etching (RIE) or a combination of these or other suitable methods. The etch rate of SiOC film can be significantly increased by using magnetron enhanced RIE.

GaN and GaAlN Gate Material Embodiments

In one embodiment, the present invention provides a DEAPROM having a memory cell **110** including a FET **200** having an at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, nanocrystalline, or combination thereof) gallium nitride (GaN) or gallium aluminum nitride (GaAlN) floating gate **215**. For example, one embodiment of a memory storage element having a GaN or GaAlN floating gate **215** is described in Forbes et al. U.S. Patent application serial number _______________ entitled DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE, filed on the same day as the present patent application, and which disclosure is herein incorporated by reference.

In one embodiment, a composition v of a polycrystalline $Ga_{1-v}Al_vN$ floating gate **215** is selected approximately between $0 < v < 1$ to obtain a desired barrier energy, as described below. The GaAlN floating gate **215** provides a lower electron affinity than polysilicon. The GaAlN floating gate **215** electron affinity can be approximately between $0.6\ eV < \chi_{215} < 2.7\ eV$ as the GaAlN composition variable v is decreased from 1 to 0. See V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996). As a result, the GaAlN floating gate **215** provides a smaller resulting barrier energy Φ_{GI} than a polysilicon gate material having an electron affinity $\chi_{215} \approx 4.2\ eV$. For example, using a SiO_2 gate insulator **225**, a barrier energy approximately between $-0.3\ eV < \Phi_{GI} < 1.8\ eV$ is obtained using an GaAlN floating gate **215** as the GaAlN composition v varies between $v \approx 1$ (i.e., approximately AlN) and $v \approx 0$ (i.e., approximately GaN). By contrast, a conventional polysilicon floating gate material provides a barrier energy $\Phi_{GI} \approx 3.3\ eV$ at an interface with an SiO_2 gate insulator **225**.

In one embodiment, substrate **230** is bulk silicon, although other bulk semiconductor and semiconductor-on-insulator (SOI) materials could also be used for substrate **230** such as, for example, sapphire, gallium arsenide (GaAs), GaN, AlN, and diamond. In one embodiment, gate insulator **225** is SiO_2, although other dielectric materials could also be used for gate insulator **225**, as described above, such as

amorphous insulating GaN (a-GaN), and amorphous insulating AlN (a-AlN). The FET **200** using a GaAlN floating gate **215** has mobility and turn-on threshold voltage (V_T) magnitude parameters that are advantageously influenced less by charge at SiO_2-GaAlN interface surface states than at a conventional SiO_2-polysilicon interface.

In one embodiment floating gate **215** is formed of a polycrystalline, microcrystalline, or nanocrystalline, GaN thin film that is CVD deposited on a thin (e.g., 500 Å thick) AlN buffer layer, such as by metal organic chemical vapor deposition (MOCVD), which advantageously yields improved crystal quality and reduced microscopic fluctuation of crystallite orientation. See e.g., V. M. Bermudez et al. "The Growth and Properties of Al and AlN films on GaN" J. Appl. Physics, Vol. 79, No. 1, pp. 110-119 (1996). See also I. Akasaki et al. "Effects of AlN Buffer Layer on Crystallographic Structure and On Electrical and Optical Properties of GaN and $Ga_{1-x}Al_xN$ Films Grown on Sapphire Substrate by MOVPE," J. Of Crystal Growth, Vol. 98, pp. 209-19, North Holland, Amsterdam (1989).

In one embodiment, floating gate **215** is formed from a GaN film grown in a horizontal reactor operating at atmospheric pressure. Trimethyl gallium (TMG), trimethylaluminum (TMA), and ammonia (NH_3) are used as source gases, and hydrogen (H_2) is used as a carrier gas. The TMG, TMA, and NH_3 are mixed just before the reactor, and the mixture is fed at high velocity (e.g., 110 cm/s) to a slanted substrate **230** through a delivery tube. The desired GaAlN composition v is obtained by controlling the concentration ratio of TMG to TMA. In one embodiment, a 500 Å AlN buffer layer is obtained by growth at 600 degrees Celsius at a deposition rate of 100 Å/minute for approximately 5 minutes, then a epitaxial crystalline or polycrystalline layer of GaN is deposited at 1000 degrees Celsius.

In another embodiment plasma-enhanced molecular beam epitaxy (PEMBE) is used to form a GaN or GaAlN floating gate **215**, for example, by using electron cyclotron resonance (ECR) plasma during molecular beam epitaxy (MBE). The background pressure in the MBE chamber is typically less than 10^{-10} torr. Ga flux (e.g., 99.99999% pure) is supplied by a conventional Knudsen effusion cell. The

semiconductor substrates **230** are heated to a temperature of approximately 850 degrees Celsius, and exposed to a nitrogen plasma (e.g., 35 Watt plasma power level) to clean the surface of the substrate **230** and form a thin AlN layer thereupon. The temperature is then lowered to approximately 550 degrees Celsius for growth of a thin (e.g., 300 Å) GaN buffer layer (e.g., using 20 Watt plasma power level for growth in a low active nitrogen overpressure environment). The temperature is then increased, such as to approximately 800 degrees Celsius, to form the remainder of the GaN or GaAlN film forming floating gate **225**, such as at a deposition rate of approximately 0.22 microns/hour.

Conclusion

The present invention provides a DEAPROM cell. The memory cell has a floating electrode, such as a floating gate electrode in a floating gate field-effect transistor. According to one aspect of the invention, a barrier energy between the floating electrode and the insulator is lower than the barrier energy between polysilicon and SiO_2, which is approximately 3.3 eV. The memory cell also provides large transconductance gain, which provides a more easily detected signal and reduces the required data storage capacitance value. According to another aspect of the invention, the shorter retention time of data charges on the floating electrode, resulting from the smaller barrier energy, is accommodated by refreshing the data charges on the floating electrode. By decreasing the data charge retention time and periodically refreshing the data, the write and erase operations can be several orders of magnitude faster. In this respect, the memory operates similar to a memory cell in DRAM, but avoids the process complexity, additional space needed, and other limitations of forming stacked or trench DRAM capacitors.

Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that the above-described embodiments can be used in combination, and any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is

intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

WHAT IS CLAIMED IS:

1. A memory cell comprising:

a storage electrode for storing charge; and

an insulator adjacent to the storage electrode, wherein a barrier energy between the insulator and the storage electrode is less than approximately 3.3 eV.

2. The memory cell of claim **1**, wherein materials comprising at least one of the storage electrode and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

3. The memory cell of claim **2**, wherein the barrier energy is selected to obtain a desired data charge retention time of less than or equal to approximately 40 seconds at 250 degrees Celsius.

4. The memory cell of claim **2**, wherein the barrier energy is selected to obtain a desired erase time of less than approximately 1 second.

5. The memory cell of claim **2**, wherein the barrier energy is selected to obtain a desired erase voltage of less than approximately 12 Volts.

6. The memory cell of claim **1**, wherein the insulator comprises a material that has a material composition that is selected to obtain a larger electron affinity than silicon dioxide.

7. The memory cell of claim **1**, wherein the storage electrode comprises a material that has a material composition that is selected to obtain a smaller electron affinity than polycrystalline silicon.

8. The memory cell of claim **1**, wherein the barrier energy is less than approximately 2.0 eV.

9. The memory cell of claim **1**, wherein the storage electrode is isolated from conductors and semiconductors.

10. The memory cell of claim **1**, wherein the storage electrode is transconductively capacitively coupled to a channel

11. A transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, wherein a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV.

12. The transistor of claim **11**, wherein materials comprising at least one of the floating gate and the insulator are selected to have an electron affinity causing the barrier energy to be selected at less than approximately 3.3 eV.

13. The transistor of claim **12**, wherein the barrier energy is selected to obtain a data charge retention time of the transistor that is adapted for dynamic refreshing of charge stored on the floating gate.

14. The transistor of claim **11**, wherein the floating gate is isolated from conductors and semiconductors.

15. The transistor of claim **11**, wherein the insulator comprises a material that has a material composition that is selected to obtain a larger electron affinity than silicon dioxide.

16. The transistor of claim **11**, wherein the floating gate includes a material that has a material composition that is selected to obtain a smaller electron affinity than polycrystalline silicon.

17. The transistor of claim **11**, further comprising a control electrode, separated from the floating gate by an intergate dielectric.

18. The transistor of claim **17**, wherein the area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than the area of a capacitor formed by the floating gate, the insulator, and the channel region

19. The transistor of claim **17**, wherein the intergate insulator has a permittivity that is higher than a permittivity of silicon dioxide.

20. The transistor of claim **11**, wherein the floating gate is capacitively separated from the channel region for providing transconductance gain.

21. A method of using a floating gate transistor having a barrier energy of less than approximately 3.3 eV at an interface between a floating gate electrode and an adjacent insulator, the method comprising:

storing data by changing the charge of the floating gate;

reading data by detecting a current between a source and a drain; and

refreshing data based on a data charge retention time that depends upon the barrier energy.

22. The method of claim **21**, wherein storing data by changing the charge of the floating gate transconductively provides an amplified signal between the source and the drain.

23. The method of claim **21**, wherein the detected current is based on the charge of the floating gate and a transconductance gain of the floating gate transistor.

24. A method of forming a floating gate transistor, the method comprising:

forming source and drain regions;

selecting floating gate and gate insulator materials such that a barrier energy at an interface therebetween is less than approximately 3.3 eV;

forming a gate insulator from the gate insulator material; and

forming a floating gate from the gate material, such that the floating gate is isolated from conductors and semiconductors.

25. The method of claim **24**, wherein selecting the floating gate and gate insulator materials is based on a desired data charge retention time of less than or equal to approximately 40 seconds at 250 degrees Celsius.

26. The method of claim **25**, wherein the data charge retention time is based on refreshing charge stored on the floating gate.

27. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, wherein an interfacial barrier energy between the floating gate and the insulator is less than approximately 3.3 eV; and

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric.

08/902133

DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY AND METHODS OF FABRICATION AND USE

Abstract of the Disclosure

A floating gate transistor has a reduced barrier energy at an interface with an adjacent gate insulator, allowing faster charge transfer across the gate insulator at lower voltages. Data is stored as charge on the floating gate. The data charge retention time on the floating gate is reduced. The data stored on the floating gate is dynamically refreshed. The floating gate transistor provides a dense and planar dynamic electrically alterable and programmable read only memory (DEAPROM) cell adapted for uses such as for a dynamic random access memory (DRAM) or a dynamically refreshed flash EEPROM memory. The floating gate transistor provides a high gain memory cell and low voltage operation.

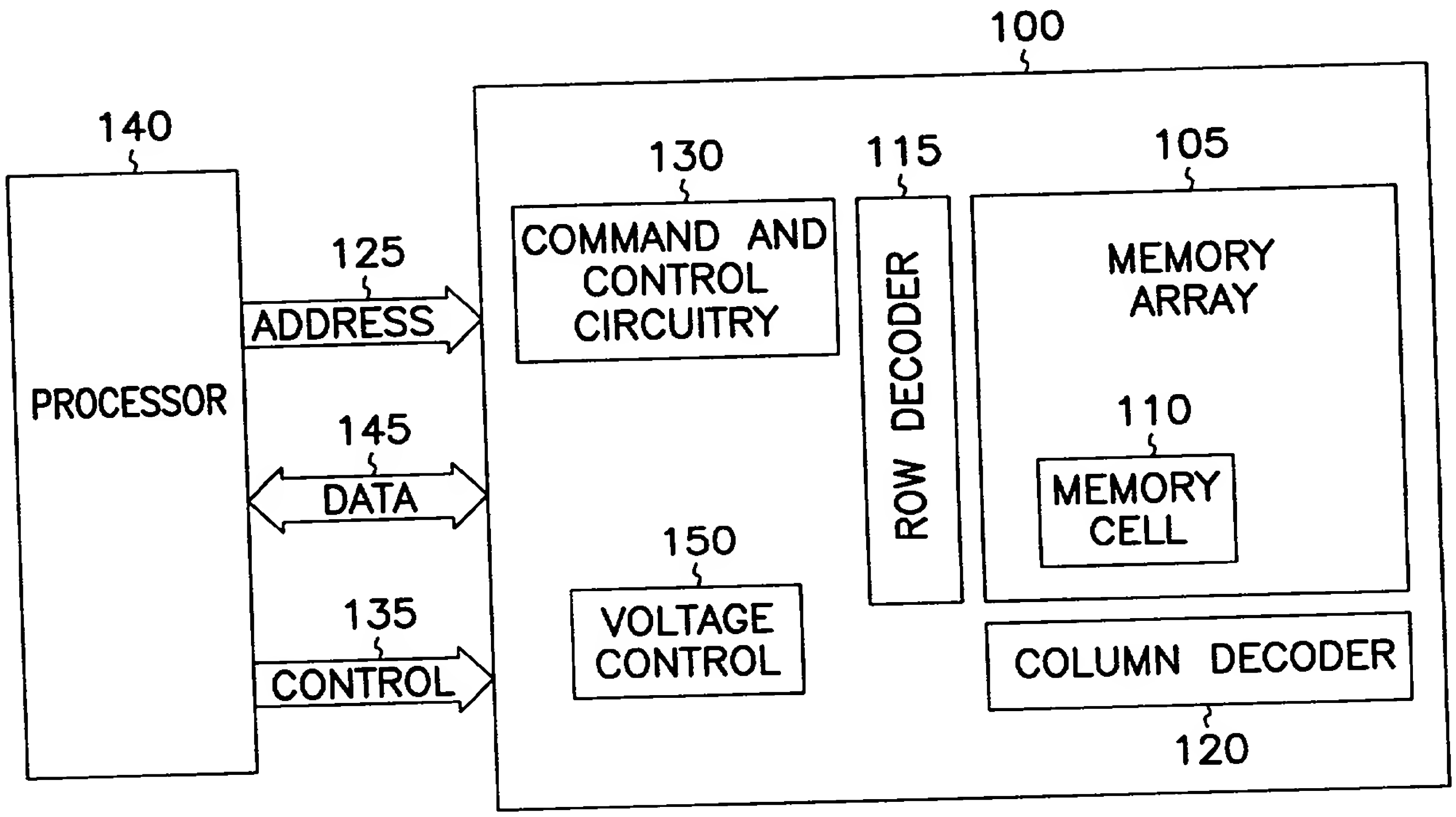
100
140
PROCESSOR
125
ADDRESS
145
DATA
135
CONTROL
130
COMMAND AND CONTROL CIRCUITRY
115
ROW DECODER
105
MEMORY ARRAY
110
MEMORY CELL
150
VOLTAGE CONTROL
COLUMN DECODER
120

FIG. 1

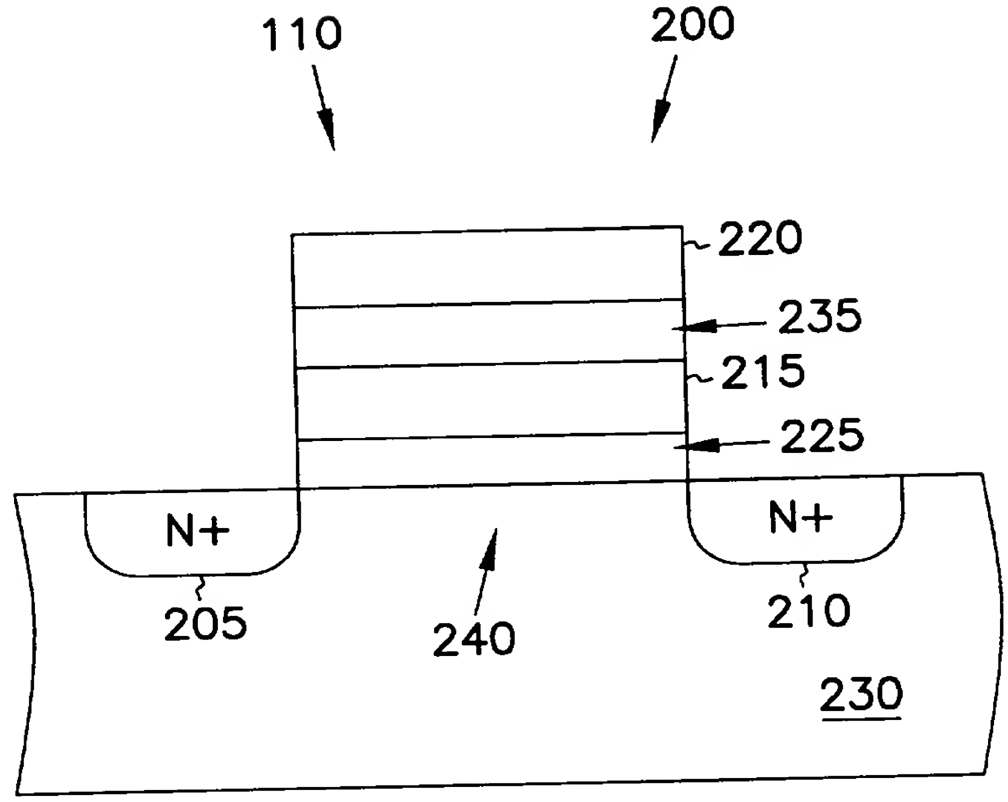
110
200
220
235
215
225
N+
N+
205
240
210
230

FIG. 2

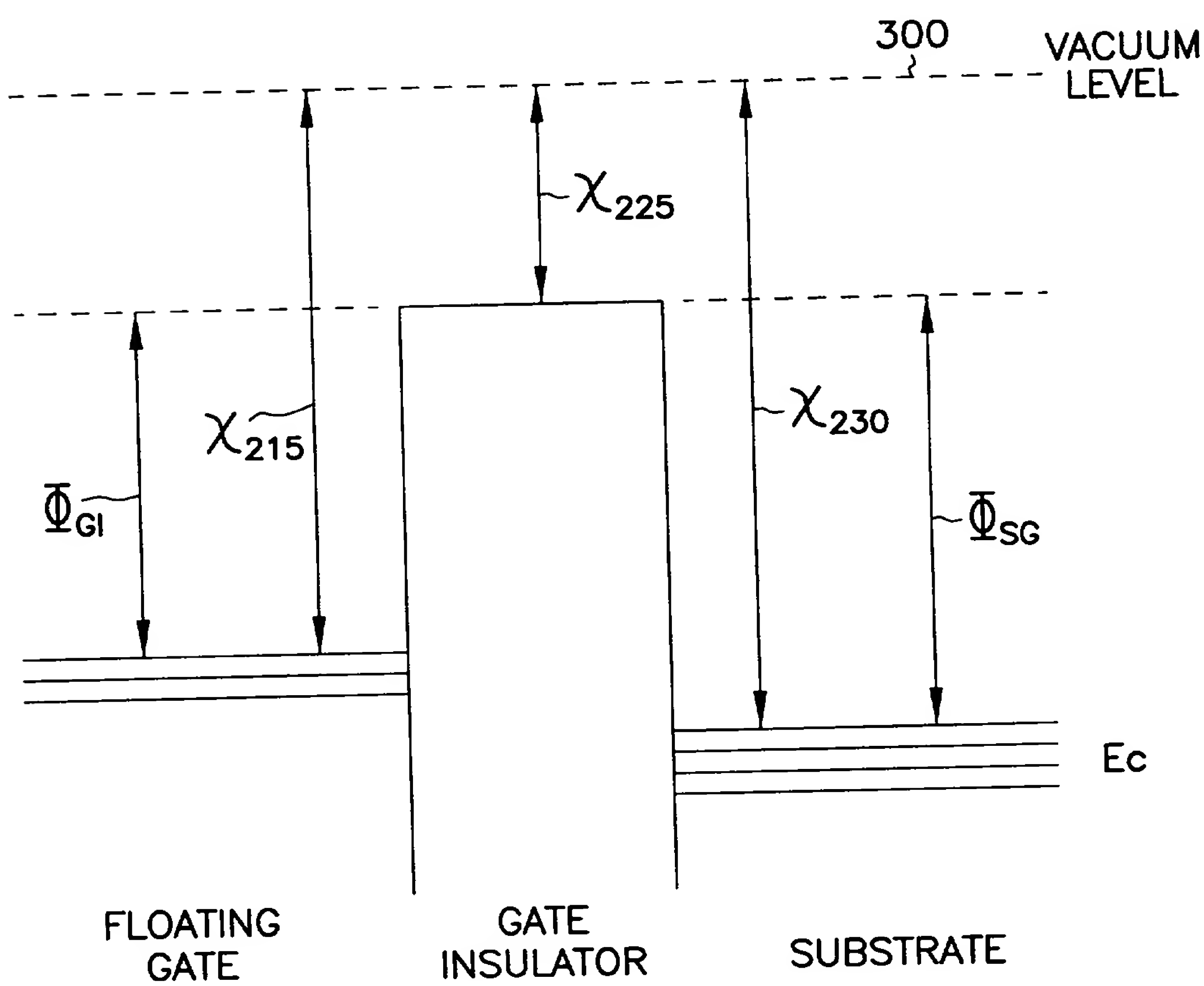
300
VACUUM
LEVEL
χ_{225}
χ_{215}
Φ_{GI}
χ_{230}
Φ_{SG}
Ec
FLOATING
GATE
GATE
INSULATOR
SUBSTRATE

FIG. 3

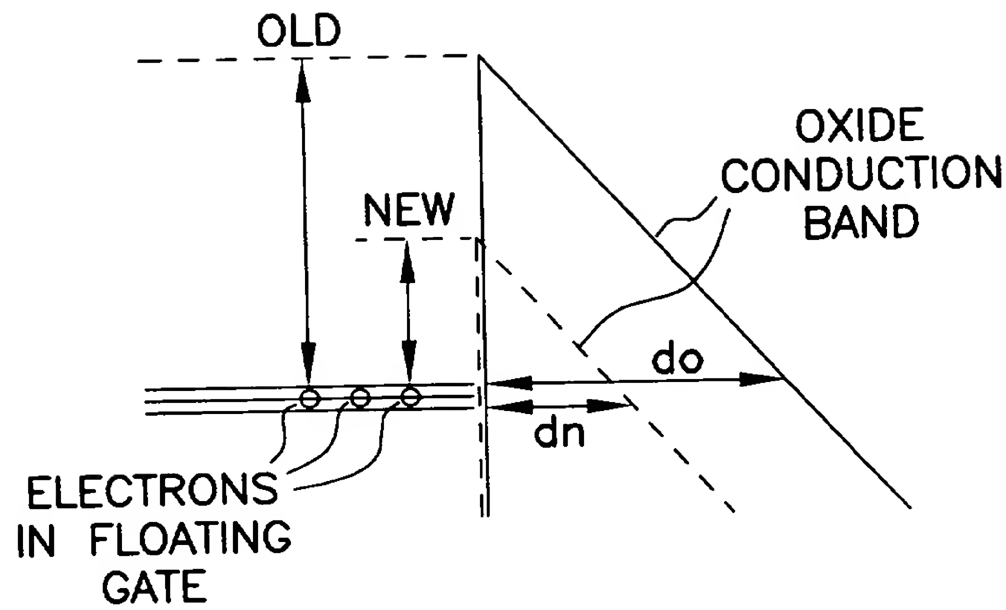
OLD
NEW
OXIDE
CONDUCTION
BAND
do
dn
ELECTRONS
IN FLOATING
GATE

FIG. 4

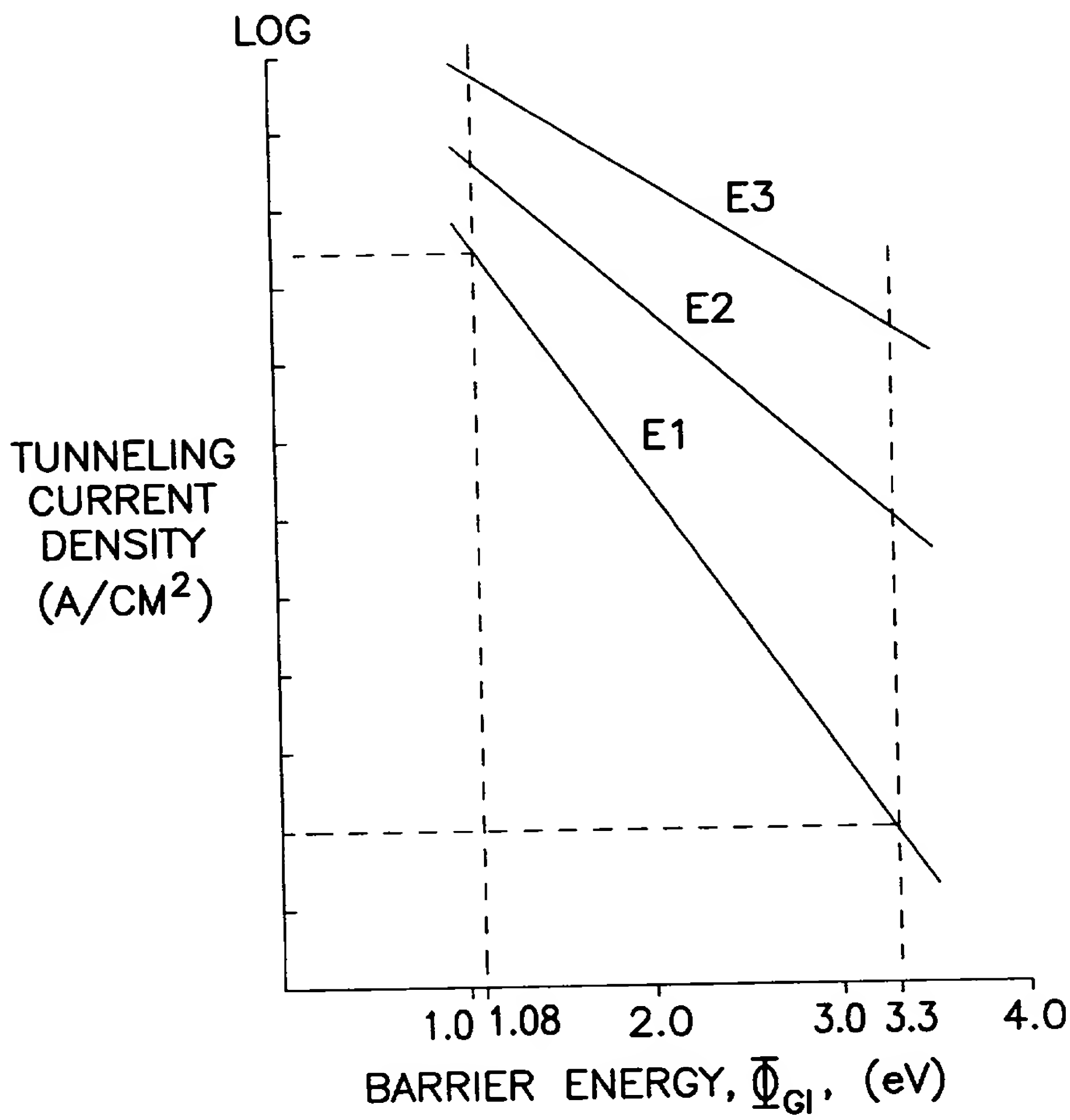
LOG
TUNNELING
CURRENT
DENSITY
(A/CM2)
E3
E2
E1
1.0
1.08
2.0
3.0
3.3
4.0
BARRIER ENERGY, Φ_{GI}, (eV)

FIG. 5

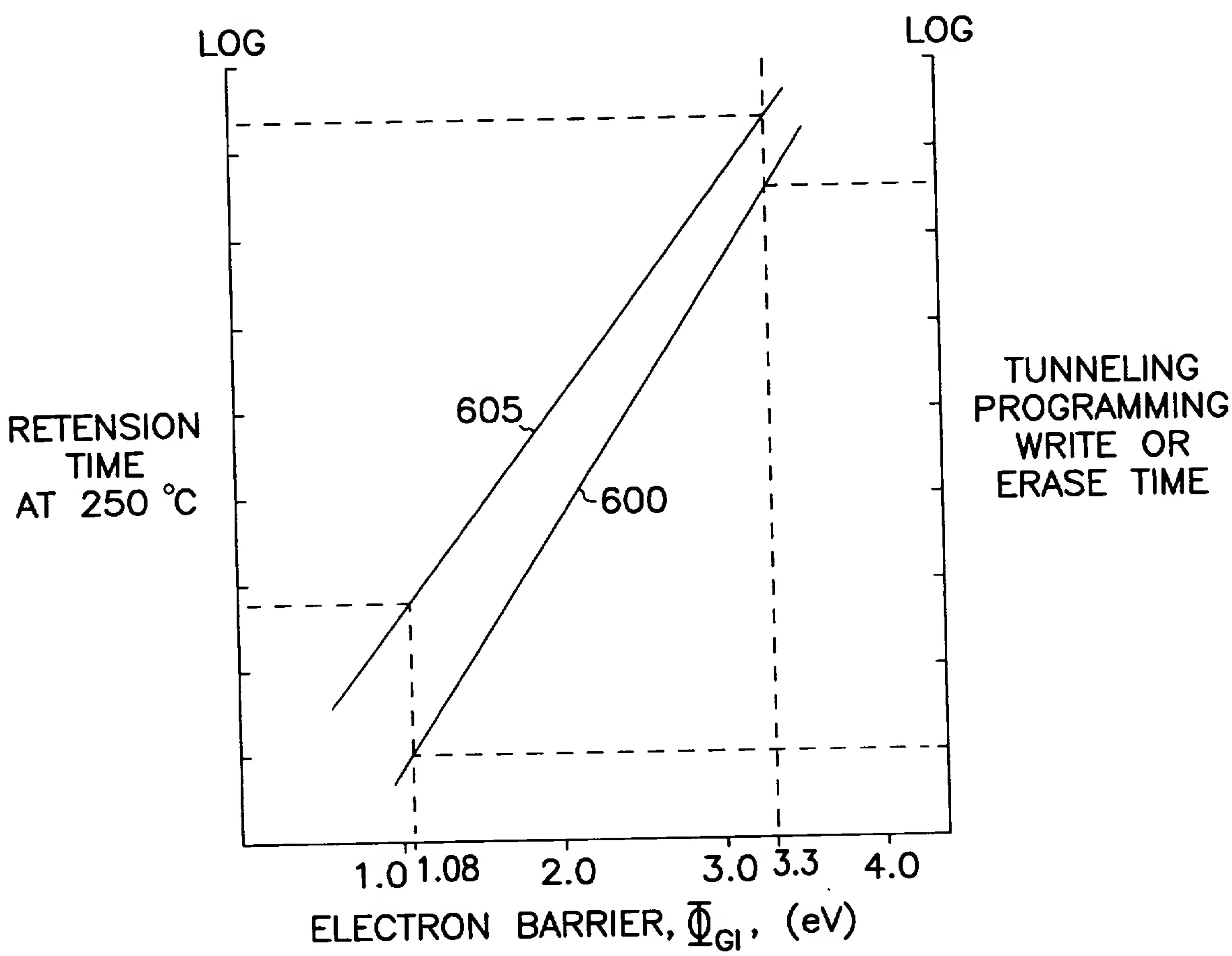
LOG
LOG
RETENSION
TIME
AT 250 °C
605
600
TUNNELING
PROGRAMMING
WRITE OR
ERASE TIME
1.0
1.08
2.0
3.0
3.3
4.0
ELECTRON BARRIER, Φ_{GI}, (eV)

FIG. 6

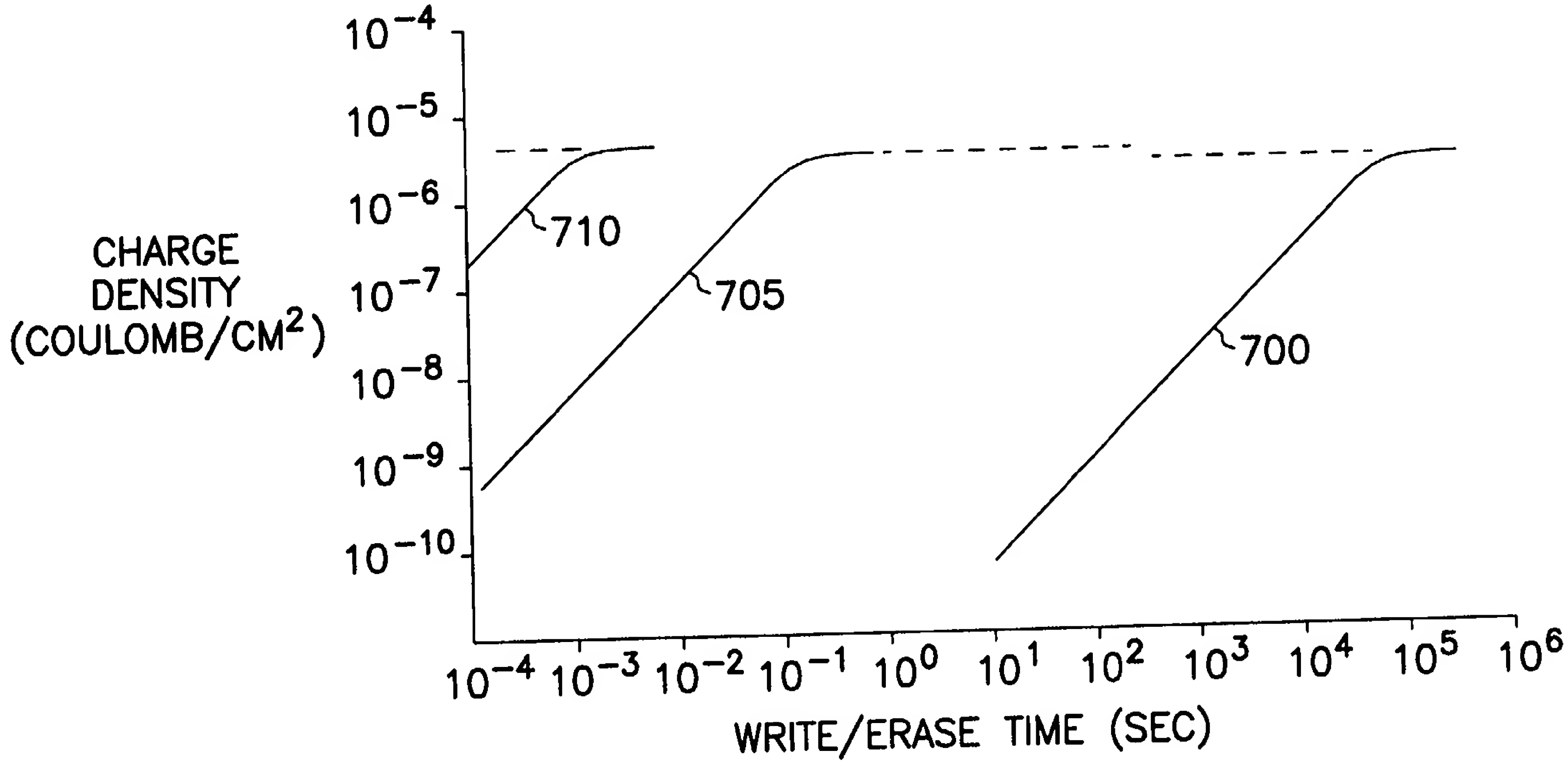
CHARGE DENSITY (COULOMB/CM^2)
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
710
705
700
10^{-4} 10^{-3} 10^{-2} 10^{-1} 10^{0} 10^{1} 10^{2} 10^{3} 10^{4} 10^{5} 10^{6}
WRITE/ERASE TIME (SEC)

FIG. 7

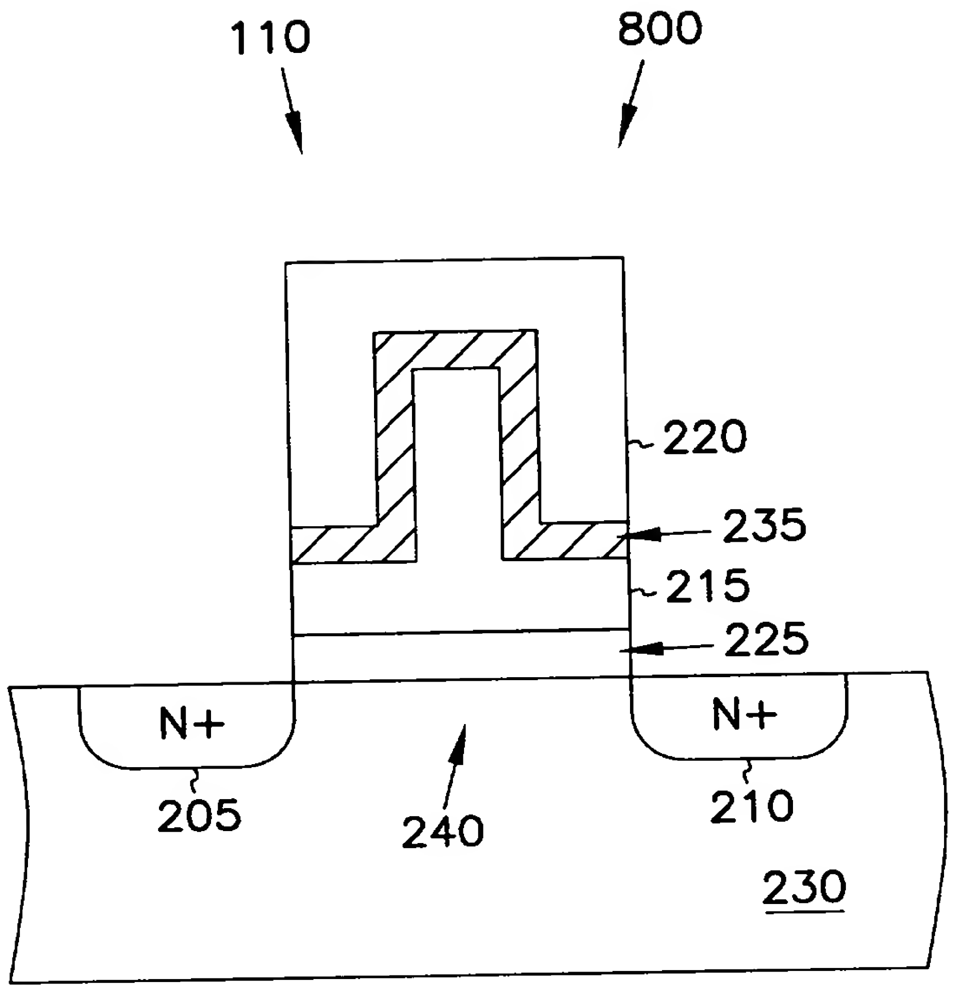

FIG. 8

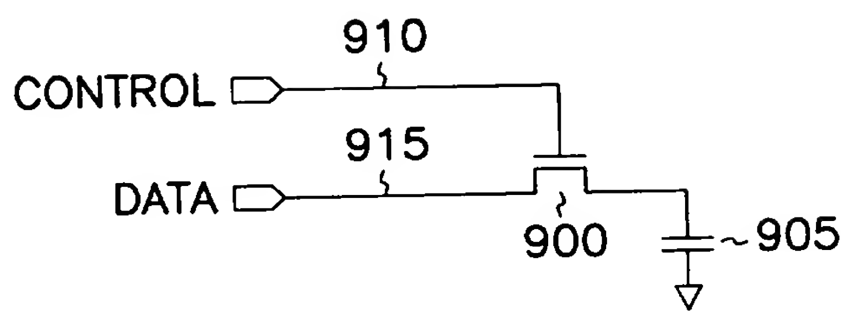

FIG. 9A (PRIOR ART)

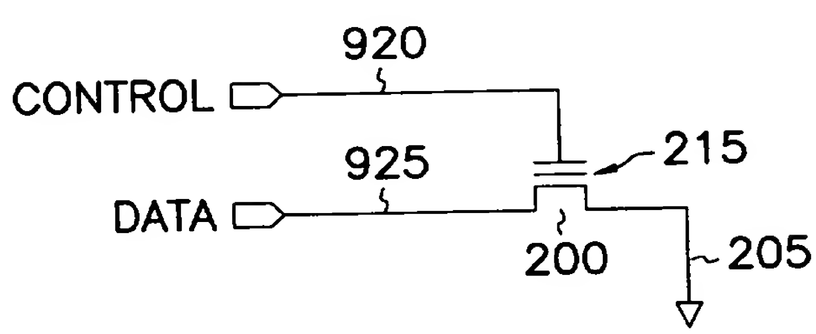

FIG. 9B

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY AND METHODS OF FABRICATION AND USE**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg No. 39,610	Forrest, Bradley A	Reg No. 30,837	Lundberg, Steven W	Reg No 30,568
Billig, Patrick G.	Reg No. 38,080	Harris, Robert J	Reg No 37,346	Lynch, Michael L	Reg No 30,871
Billion, Richard E	Reg. No 32,836	Hofmann, Rudolph P., Jr.	Reg. No 38,187	Pappas, Lia M	Reg No 34,095
Brennan, Thomas F.	Reg. No 35,075	Holloway, Sheryl S	Reg No 37,850	Schwegman, Micheal L	Reg No 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I	Reg. No. 40,052	Simboli, Paul B.	Reg No 38,616
Dryja, Michael A.	Reg No 39,662	Kluth, Daniel J.	Reg. No 32,146	Slifer, Russell D	Reg No. 39,838
Embretson, Janet E	Reg. No. 39,665	Lemaire, Charles A	Reg No 36,198	Viksnins, Ann S	Reg. No. 37,748
Farney, W Bryan	Reg. No. 32,651	Litman, Mark A	Reg No 26,390	Woessner, Warren D	Reg No 30,440
Fogg, David N.	Reg No. 35,138				

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)373-6900

Our Ref. 303.356US1
Title: Dynamically Electrically Alterable Programmable Read Only Memory
Filing Date: Herewith

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: ______________________ Date: ______________
Leonard Forbes

Full Name of joint inventor number 2 : **Joseph E. Geusic**
Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: Joseph E Geusic Date: 7/25/97
Joseph E. Geusic

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: ______________________ Date: ______________

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: ______________________ Date: ______________

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

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Corvallis, OR 97330

Signature: Leonard Forbes Date: 24 Jul 97
Leonard Forbes

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Citizenship: **United States of America** Residence: **Berkeley Heights, NJ**
Post Office Address: 261 Lorraine Drive
Berkeley Heights, NJ 07922

Signature: Date:
Joseph E. Geusic

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: Date:

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: Date:

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(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.